AMENDMENTS TO THE CLAIMS

This Listing of Claims replaces all prior versions, and listings, of claims in this application.

1. (Currently Amended) A method comprising:

a host transmitting a first signal to a first device coupled with a second device;

in response to the first signal, the second device transmitting a second signal transmitted to the host prior to transmission of a third signal from the first device to the host in a handshake initialization sequence, the second device to consecutively transmit the second signal and the third signal to the host;

the host detecting a presence of the second device, in response to receipt of the second signal if the host is of a first set of hosts; and

the host ignoring the second signal if the host is of a second set of hosts.

2. (Original) The method of claim 1, wherein the second device is a fail over switch.

3. (Previously Presented) The method of claim 1, further comprising:

the host transmitting the second signal to the first device; and

the host receiving a second signal from the first device.

4. (Original) The method of claim 1, performed during a handshake initialization sequence between the host and the first device.

5. (Original) The method of claim 3, wherein the second signal is a Serial ATA out of band (OOB) signal.

6. (Original) The method of claim 2, wherein the fail-over switch is a Serial ATA fail over switch.

7. (Currently Amended) A machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

a host transmitting a first signal to a first device coupled with a second device~~, the second device being a fail over switch that provides two paths between the host and the first device~~;

the second device transmitting a second signal to the host prior to transmission of a third signal from the first device to the host in a handshake initialization sequence, the second device to consecutively transmit the second signal and the third signal to the host;

the host identifying a presence of the second device, in response to receipt of the second signal;

the host receiving ~~a~~ the third signal from the first device;

the host transmitting the second signal to the first device; and

the host receiving the second signal from the first device.

8. (Original) The machine-accessible medium of claim 7, wherein the operations are performed during a handshake initialization sequence between the host and the first device.

9. (Original) The machine-accessible medium of claim 7, wherein the second signal is a Serial ATA out of band (OOB) signal.

10. (Original) The machine-accessible medium of claim 7, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

11. (Currently Amended) A machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

a host transmitting a COMRESET to a device coupled with a switch;

the host receiving a COMWAKE originating from the switch prior to receiving a COMINIT from the device in a handshake initialization sequence, the switch to consecutively transmit the COMWAKE and the COMINIT to the host;

the host identifying a presence of the switch, in response to receipt of the COMWAKE;

the host receiving ~~a~~ the COMINIT from the device;

the host transmitting the COMWAKE to the device; and

the host receiving the COMWAKE from the device.

12. (Original) The machine-accessible medium of claim 11, wherein the operations are performed during a handshake initialization sequence between the host and the device.

13. (Original) The machine-accessible medium of claim 11, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

14. (Currently Amended) A system comprising:

a processor; and

a machine-accessible medium that provides instructions that, if executed by the processor, will cause the processor to perform operations comprising:

transmit a COMRESET to a device coupled with a fail over switch;

receive a COMWAKE originating from the fail over switch prior to receiving a COMINIT from the device in a handshake initialization sequence, the COMWAKE and the COMINIT to be received consecutively from the fail over switch;

identify a presence of the fail over switch, in response to receipt of the COMWAKE;

receive the~~a~~ COMINIT from the device;

transmit the COMWAKE to the device; and

receive the COMWAKE from the device.

15. (Original) The system of claim 14, wherein the fail-over switch is a Serial ATA fail over switch.

16. (Original) The system of claim 14, wherein the operations are performed during a handshake initialization sequence between the system and the device.

17. (Original) The system of claim 14, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

18. (Currently Amended) A system comprising:

a processor;

a network connection; and

a machine-accessible medium that provides instructions that, if executed by a machine, will cause said machine to perform operations comprising:

transmitting a first signal to a first device coupled with a second device~~, the second device being a fail over switch that provides two paths for the first signal to the first device~~;

~~transmitting~~ receiving a second signal ~~to the host prior to transmission of~~ and a third signal ~~from the first device~~consecutively before transmitting the second signal in a handshake initialization sequence;

identifying a presence of the second device, in response to receipt of the second signal;

~~receiving the third signal from the first device;~~

transmitting the second signal to the first device; and

receiving the second signal from the first device.

19. (Original) The system of claim 18, wherein the second device is a fail over switch.

20. (Original) The system of claim 18, wherein the operations are performed during a handshake initialization sequence between the system and the first device.

21. (Original) The system of claim 18, wherein the medium is one of an internal logic of a circuit and an internal state machine of a circuit.

22. (Currently Amended) A system comprising:

a host controller ~~that initiates~~to initiate a handshake initialization sequence;

a serial ATA device ~~that participates~~to participate in the handshake initialization sequence; and

a fail over switch ~~that provides for a first path and a second path between the host controller and the serial ATA device, the second path to be utilized when the first path fails, the fail over switch transmits~~ to consecutively transmit an out of band signal and a standard handshake signal to the host controller during the handshake initialization sequence after the host controller initiates the handshake initialization sequence and before the host controller transmits a subsequent signal to the serial ATA device, the out of band signal notifies the host controller that a switch between ~~the~~ a first path and ~~the~~ a second path of the fail over switch has occurred.